IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a continuation-in-part (CIP) application of U.S. Patent Application Serial No. 09/796,080, filed February 28, 2001, ~~pending,~~ now U.S. Patent 6,571,352 B2, issued May 27, 2003, which is a continuation of U.S. Patent Application Serial No. 09/143,283, filed August 28, 1998, issued March 6, 2001, as U.S. Patent No. 6,199,177 B1.

Please amend paragraph number **[0008]** as follows:

[0008] Unfortunately, it is difficult to provide enough redundant rows or columns in a semiconductor memory to repair all failing memory cells therein using the conventional repair process described above without using an excessive amount of space (commonly known as "real estate") in the memory for the redundant rows or columns. With the increasing size of semiconductor memories continuously increasing the need for redundancy, memory designers find themselves caught between providing sufficient redundancy to successfully repair most memories. As a ~~result~~ result, memory designers are either using excessive space in the ~~memories,~~ memories or providing insufficient redundancy to save space in the memories and, as a result, having to discard memories that are unrepairable. Obviously, neither alternative is desirable.

Please amend paragraph number **[0035]** as follows:

[0035] The compare signals CMP(0:7) also include the column address CA(0:7) as shown in Table 2. The compare circuitry 104 compares the compare signals CMP(0:7) to the bad address BA(0:7). If there is no match, the column address CA(0:7) is used to select a column of the array 96 and the row decoder 106 selects a row address. When a match occurs, a column is selected by a column decoder 110 in accordance with redundant decode signals DEC(0:7) that are output by the mux circuitry 100 as shown in Table 3, below.

Table 3

S(0:7)	DEC7	DEC6	DEC5	DEC4	DEC3	DEC2	DEC1	DEC0
0	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
1	CA0	CA1	CA2	CA3	CA4	CA5	CA6	RA0
3	CA0	CA1	CA2	CA3	CA4	CA5	RA1	RA0
7	CA0	CA1	CA2	CA3	CA4	RA2	RA1	RA0
15	CA0	CA1	CA2	CA3	RA3	RA2	RA1	RA0
31	CA0	CA1	CA2	RA4	RA3	RA2	RA1	RA0
63	CA0	CA1	RA5	RA4	RA3	RA2	RA1	RA0
127	CA0	RA6	RA5	RA4	RA3	RA2	RA1	RA0
255	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0